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L7: Entry 9 of 9 File: USPT Sep 15, 1992

US-PAT-NO: 5148545
DOCUMENT-IDENTIFIER: US 5148545 A

TITLE: Bus device which performs protocol confidential transactions

DATE-ISSUED: September 15, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Herbst; William C.	Franklin	MA		
Baker; Lauren D.	Westford	MA		
Stevens; Gary W.	Whitinsville	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Clearpoint Research Corporation	Hopkinton	MA			02

APPL-NO: 07/ 384128 [PALM]
DATE FILED: July 21, 1989

INT-CL: [05] G06F 13/36, G06F 12/14

US-CL-ISSUED: 395/725; 364/DIG.1, 364/240.8, 364/240.1, 364/242.92, 364/246
US-CL-CURRENT: 710/240

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 395/725

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3993981	November 1976	Cassarino, Jr. et al.	364/200
☐	4136400	January 1979	Carwell et al.	364/900
☐	4371925	February 1983	Carberry et al.	364/200
☐	4706190	November 1987	Bomba et al.	364/200
☐	5001624	March 1991	Hoffman et al.	364/200

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ART-UNIT: 237

PRIMARY-EXAMINER: Chan; Eddie P.

ATTY-AGENT-FIRM: Porter; Edward W.

ABSTRACT:

A bus device of a first type uses a first arbitration protocol. The first-type device is designed for use in a computer system having a communications bus, and one or more other bus devices connected to the bus, including possible first-type bus devices which also use the first arbitration protocol and one or more second-type bus devices which use a second, different, arbitration protocol. The first-type bus device includes a protocol specific memory for storing information; means for monitoring the bus to determine whether the current bus master of the bus arbitrated in the manner of the first or second arbitration protocols; and means for denying the current bus master the ability to access information stored in the protocol specific memory if the means for monitoring determines the bus master arbitrated according to the second arbitration protocol.

3 Claims, 63 Drawing figures

US-PAT-NO: 5970234

DOCUMENT-IDENTIFIER: US 5970234 A

TITLE: PCI bus arbiter and a bus control system having the same

---------- KWIC ---------

Brief Summary Text - BSTX (14):

The bus control system of present invention may include a central processing unit having functions of processing or manipulating data which are inputted to a computer system, a first PCI bus bridge which changes structure of signals from the bus masters to be suitable for a first PCI bus a second PCI bus bridge which changes structure of signals from the bus masters to be suitable for a second PCI bus, and an EISA/ISA bus bridge which changes structure of signals from the bus masters to be suitable for an EISA/ISA bus. The bus control system may also include a first arbiter in a main chip set which receives first request signals requesting an authority to use the first PCI bus from the bus masters, and selects a first bus master from the bus masters, and produces a first grant signal to authorize the first bus master to use the first PCI bus. The bus control system can include a second arbiter which receives second request signals requesting an authority to use the second PCI bus from the bus masters, and selects a second bus master from the bus masters, and produces a second grant signal to authorize the second bus master to use the second PCI bus.

US005970234A

United States Patent [19]

Jin

[11] Patent Number: 5,970,234

[45] Date of Patent: Oct. 19, 1999

[54] **PCI BUS ARBITER AND A BUS CONTROL SYSTEM HAVING THE SAME**

[75] Inventor: Sung-Kon Jin, Uiwang-si, Rep. of Korea

[73] Assignee: SamSung Electronics Co., Ltd., Suwon, Rep. of Korea

[21] Appl. No.: 08/792,424

[22] Filed: Jan. 30, 1997

[30] Foreign Application Priority Data

Jan. 30, 1996 [KR] Rep. of Korea 96-2136

[51] Int. Cl.[6] G06F 13/36; G06F 13/37

[52] U.S. Cl. 395/291; 395/728; 395/731; 395/308

[58] Field of Search 395/287, 291, 395/294, 296, 307, 303, 306, 308, 309, 728, 732

[56] References Cited

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5,594,882	1/1997	Bell	711/212
5,608,884	3/1997	Potter	395/309
5,630,145	5/1997	Chen	395/750.04

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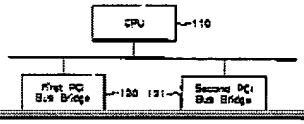
Bit 3 Computer Corporation, Product Summary, Jan. 1997, pp. 6 and 7 including cover page.

Primary Examiner—Ayaz R. Sheikh
Assistant Examiner—Xuong M. Chung-Trans
Attorney, Agent, or Firm—Robert E. Bushnell, Esq.

[57] ABSTRACT

A PCI bus arbiter is provided as an additional PCI bus in PCI peer-to-peer bus bridge system. A bus control system having the PCI bus arbiter is also provided. The bus control system includes bus masters, a first PCI bus bridge, a second PCI bus bridge, an EISA/ISA bus bridge for changing structures of signals from the bus masters to be suitable for corresponding bus, a first arbiter in a main chip set, and a second arbiter for arbitration process. The second arbiter includes an edge detecting state machine which detects whether a PCI bus is accessed by a bus master, and produces a frame-signal which changes a logic state thereof according to an access condition of the PCI bus. The second arbiter may also include a priority resolve state machine which receives the frame-signal and produces priority values which determine an order of bus masters to use the PCI bus, wherein the priority values are changed according to the frame-signal. The second arbiter can include a hand shake state machine which produces and outputs grant-signals to grant authority to use the PCI bus to bus masters according to the priority value.

18 Claims, 7 Drawing Sheets



US-PAT-NO: 5796413

DOCUMENT-IDENTIFIER: US 5796413 A
See image for Certificate of Correction

TITLE: Graphics controller utilizing video memory to provide macro command capability and enhanced command buffering

---------- KWIC ---------

Brief Summary Text - BSTX (5):

First, new bus protocols have been defined that are operable over very high bandwidths so that data and control signals may be transferred from the CPU to the graphics system at much faster rates. Some bus protocol known popularly as "local bus" protocols, have been defined to run with bus frequencies as high as the clock frequency of the CPU. By way of example, the Peripheral Component Interconnect ("PCI") bus is a local bus standard recently developed by Intel Corporation. Over a PCI bus, data transfer rates of up to 266 Mbytes per second are possible under optimum conditions with a 64-bit data bus. A PCI bus does not, however, always run at the CPU clock frequency.

US005796413A

United States Patent [19]

Shipp et al.

[11] Patent Number: 5,796,413

[45] Date of Patent: Aug. 18, 1998

[54] GRAPHICS CONTROLLER UTILIZING VIDEO MEMORY TO PROVIDE MACRO COMMAND CAPABILITY AND ENHANCED COMMAND BUFFERING

[75] Inventors: Ronald Anthony Shipp; Stuart Hecht, both of Houston; Patrick Allen Hankin, Austin, all of Tex.

[73] Assignee: Compaq Computer Corporation, Houston, Tex.

[21] Appl. No.: 568,167

[22] Filed: Dec. 6, 1995

[51] Int. Cl.[6] G06F 15/00

[52] U.S. Cl. 345/521; 345/516; 345/521

[58] Field of Search 395/501, 502, 395/507, 509, 511, 516, 520-522, 526, 250, 825, 872, 874, 412, 427; 345/501, 502, 507, 509, 511, 516, 520-522, 526; 711/202, 100

[56] References Cited

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5,341,347	1/1995	Gary	364/514 A
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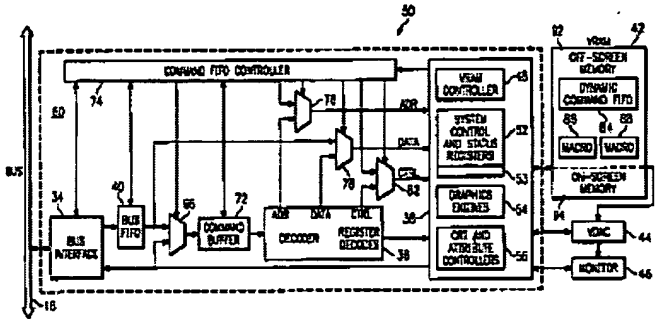
Primary Examiner—Kee M. Tung

Attorney, Agent, or Firm—Vinson & Elkins L.L.P.

[57] ABSTRACT

An apparatus and method are disclosed for buffering graphics commands in a video graphics system, and for implementing graphics macro commands. The invention makes use of off-screen portions of video memory to create a dynamic command FIFO for commands, and to store command sequences for later or repeated use ("macros"). A command FIFO controller is provided, along with an on-chip bus FIFO and an on-chip command buffer (which is also a FIFO). Several multiplexers are also provided, so as to enable the command FIFO controller to create several different paths for commands coming into the graphics controller. Incoming commands may be routed to the command executive circuitry in several different ways: through the bus FIFO and command buffer to the command execution circuitry, directly to the command execution circuitry by bypassing the bus FIFO and command buffer, or from the bus FIFO into video memory to be stored in a dynamic command FIFO and later retrieved and sent into the command buffer. The command FIFO controller is also provided with macro address generation logic for providing read pointers to macros stored in video memory, read and write address generation logic for accessing the dynamic command FIFO stored in video memory, status generation logic for use in controlling the dynamic command FIFO, and busy status logic for use in software synchronization.

23 Claims, 11 Drawing Sheets



US-PAT-NO: 6643819

DOCUMENT-IDENTIFIER: US 6643819 B1

TITLE: Hybrid root-finding technique

---------- KWIC ---------

Detailed Description Text - DETX (56):

Although the hybrid root finding mechanism has been described within the context of the data storage system 10 as shown in FIG. 1, other system implementations and operations are contemplated. For example, and with reference to FIG. 6, a computer system 150 (e.g., a PC) includes a CPU 152 coupled to a memory 154 by a memory bus 156 and connected to peripheral device such as a drive unit (e.g., a disk drive unit as shown) 158 via a local bus 160 and perhaps additional bus-to-bus bridge logic (not shown). The local bus 160 may conform to standard local bus protocols, e.g., SCSI, PCI or AT Attachment (ATA). The drive unit 158 includes a bus interface 161 for receiving data from and transferring data to the CPU 152 or memory 154. The bus interface 161 is compliant with the protocols of the local bus 160. For example, the bus interface may be an ATA bus interface, and the drive unit therefore an ATA-compliant device. The drive unit 158 further includes an intelligent controller 162 for reading data from and writing data to a disk 164, as well as the encoder 32 (FIG. 1) for encoding data to be stored on the disk and the decoder 34 (FIG. 1) employing the hybrid root-finding mechanism described above to decode encoded data read from the disk.

US-PAT-NO: 6643819

DOCUMENT-IDENTIFIER: US 6643819 B1

TITLE: Hybrid root-finding technique

---------- KWIC ---------

Detailed Description Text - DETX (56):

Although the hybrid root finding mechanism has been described within the context of the data storage system 10 as shown in FIG. 1, other system implementations and operations are contemplated. For example, and with reference to FIG. 6, a computer system 150 (e.g., a PC) includes a CPU 152 coupled to a memory 154 by a memory bus 156 and connected to peripheral device such as a drive unit (e.g., a disk drive unit as shown) 158 via a local bus 160 and perhaps additional bus-to-bus bridge logic (not shown). The local bus 160 may conform to standard local bus protocols, e.g., SCSI, PCI or AT Attachment (ATA). The drive unit 158 includes a bus interface 161 for receiving data from and transferring data to the CPU 152 or memory 154. The bus interface 161 is compliant with the protocols of the local bus 160. For example, the bus interface may be an ATA bus interface, and the drive unit therefore an ATA-compliant device. The drive unit 158 further includes an intelligent controller 162 for reading data from and writing data to a disk 164, as well as the encoder 32 (FIG. 1) for encoding data to be stored on the disk and the decoder 34 (FIG. 1) employing the hybrid root-finding mechanism described above to decode encoded data read from the disk.

US-PAT-NO: 5680556

DOCUMENT-IDENTIFIER: US 5680556 A

TITLE: Computer system and method of operation thereof wherein a BIOS ROM can be selectively locatable on diffeent buses

---------- KWIC ---------

Claims Text - CLTX (3):
b) a processor local bus connected to the processor and having a local bus protocol;

US005680556A

United States Patent [19]

Begun et al.

[11] Patent Number: 5,680,556

[45] Date of Patent: Oct. 21, 1997

[54] **COMPUTER SYSTEM AND METHOD OF OPERATION THEREOF WHEREIN A BIOS ROM CAN BE SELECTIVELY LOCATABLE ON DIFFEENT BUSES**

[75] Inventors: **Ralph Murray Begun**, Raleigh, N.C.; **William Robert Greer**, Waterville; **Christopher Michael Herring**, Essex Junction, both of Vt.

[73] Assignee: **International Business Machines Corporation**, Armond, N.Y.

[21] Appl. No.: **706,934**

[22] Filed: **Sep. 3, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 387,383, Feb. 13, 1995, abandoned, which is a continuation of Ser. No. 152,221, Nov. 12, 1993, abandoned.

[51] Int. Cl.[6] G06F 13/00

[52] U.S. Cl. 395/311; 395/306; 395/830; 395/652

[58] Field of Search 395/280, 281, 395/287, 306, 309, 311, 401, 442, 828, 830, 831, 833, 834, 858, 860, 863, 728, 653, 651, 652

[56] **References Cited**

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Primary Examiner—Parshotam S. Lall
Assistant Examiner—Viet Vu
Attorney, Agent, or Firm—Bernard D. Bogdon

[57] **ABSTRACT**

A personal computer system is provided which includes a CPU, with the CPU being operable by a BIOS including initialization or booting instructions. The system includes a local bus and a peripheral bus. A bus interface chip, including a memory controller/peripheral bus host bridge (MC/PBHB) interconnects the local bus and the peripheral bus, and includes a latch which includes as its input clock cycles generated by the CPU. The initialization instructions of the BIOS are contained in a non-volatile ROM module located to write onto either the local bus or the peripheral bus. The MC/PBHB unit is able to decode and handle ROM cycles and is configured to either pass or not pass ROM read cycles depending upon certain control states that identify whether the ROM is located on the local bus or the peripheral bus. Logic is provided to detect during the first ROM CPU cycle whether the ROM is on the peripheral bus or on the local bus, and the MC/PBHB will then either pass the signal to the peripheral bus if that is where the ROM is located, or will not pass it—in which case the local bus controller will take over and read the ROM which must be located on the local bus since it is not located on the peripheral bus.

6 Claims, 4 Drawing Sheets